

Programmable Delay Chip

The MC10E/100E195 is a programmable delay chip (PDC) designed primarily for clock de-skewing and timing adjustment. It provides variable delay of a differential ECL input transition.

The delay section consists of a chain of gates organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays the device will operate at frequencies of >1.0 GHz while maintaining over 600 mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, that is selectable entirely from a digital input allowing for very accurate system clock timing.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

- 2.0ns Worst Case Delay Range
- ≈ 20 ps/Delay Step Resolution
- >1.0GHz Bandwidth
- On Chip Cascade Circuitry
- Extended 100E V_{EE} Range of -4.2 to -5.46V
- 75K Ω Input Pulldown Resistors

PIN NAMES

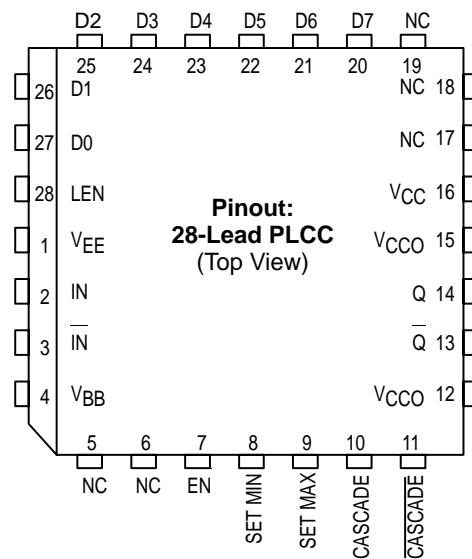
Pin	Function
IN/IN	Signal Input
EN	Input Enable
D[0:7]	Mux Select Inputs
Q/Q	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal

**MC10E195
MC100E195**

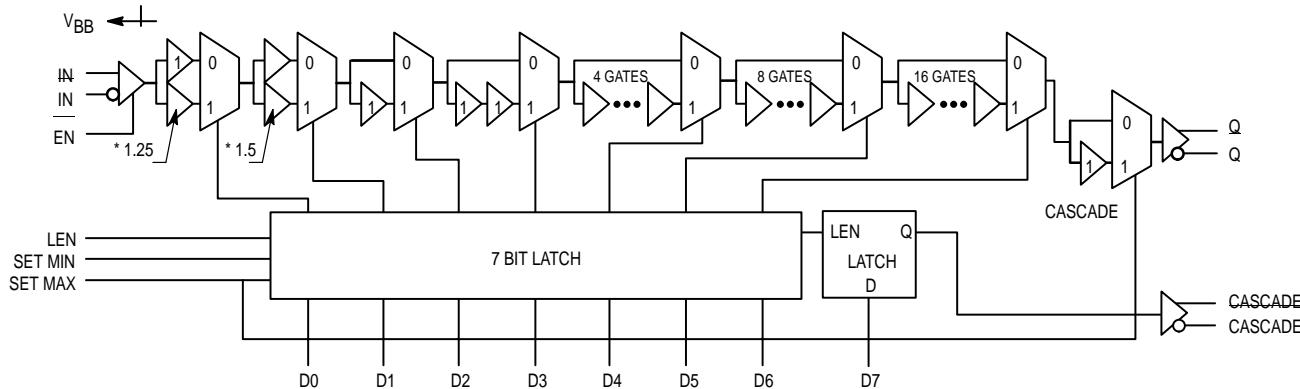
**PROGRAMMABLE
DELAY CHIP**



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02



LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN
STANDARD (STANDARD = 80 PS)



DC CHARACTERISTICS ($V_{EE} = V_{EE(\min)} \text{ to } V_{EE(\max)}$; $V_{CC} = V_{CCO} = GND$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current 10E 100E		130 130	156 156		130 130	156 156		130 150	156 179	mA	

AC CHARACTERISTICS ($V_{EE} = V_{EE(\min)} \text{ to } V_{EE(\max)}$; $V_{CC} = V_{CCO} = GND$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765	ps	
t_{PHL}	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	EN to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range $t_{PD}(\max) - t_{PD}(\min)$	2000	2175		2050	2240		2375	2580		ps	
Δt	Step Delay D0 High D1 High D2 High D3 High D4 High D5 High D6 High		17 34 55 115 250 505 1000	105	55 115 250 515 325 620 1190	17.5 35 70 140 280 560 1030	105	65 140 305 620 1220	21 42 84 168 325 672 1240	120 205 380 740 1450	ps	6
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew $t_{PHL} - t_{PLH}$		± 30			± 30			± 30		ps	1
t_s	Setup Time D to LEN D to IN EN to IN	200 800 200	0		200 800 200	0		200 800 200	0		ps	2 3
t_h	Hold Time LEN to D IN to EN	500 0	250		500 0	250		500 0	250		ps	4
t_R	Release Time EN to IN SET MAX to LEN SET MIN to LEN	300 800 800			300 800 800			300 800 800			ps	5
t_{jit}	Jitter		<5.0			<5.0			<5.0		ps	8
t_r t_f	Output Rise/Fall Time 20–80% (Q) 20–80% (CASCADE)	125 300	225 450	325 650	125 300	225 450	325 650	125 300	225 450	325 650	ps	

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
3. This setup time is the minimum time that EN must be asserted prior to the next transition of IN/IN to prevent an output response greater than ± 75 mV to that IN/IN transition.
4. This hold time is the minimum time that EN must remain asserted after a negative going IN or positive going IN to prevent an output response greater than ± 75 mV to that IN/IN transition.
5. This release time is the minimum time that EN must be deasserted prior to the next IN/IN transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs D_n). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

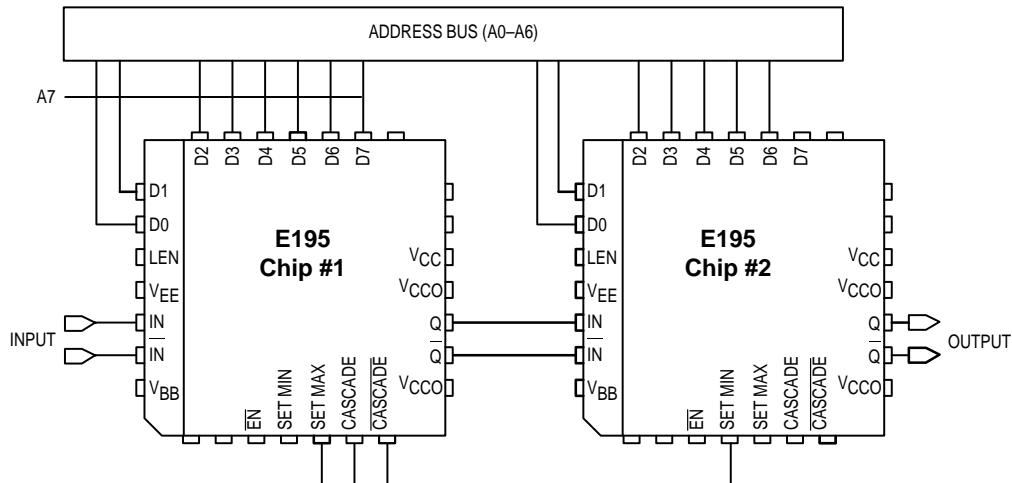


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195's

To increase the programmable range of the E195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195's without the need for any external gating. Furthermore this capability requires only one more address line per added E195. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195's. As can be seen, this scheme can easily be expanded for larger E195 chains. The D7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0-A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0-A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0-A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E195 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0-A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0-A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices one simply needs to connect the D7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

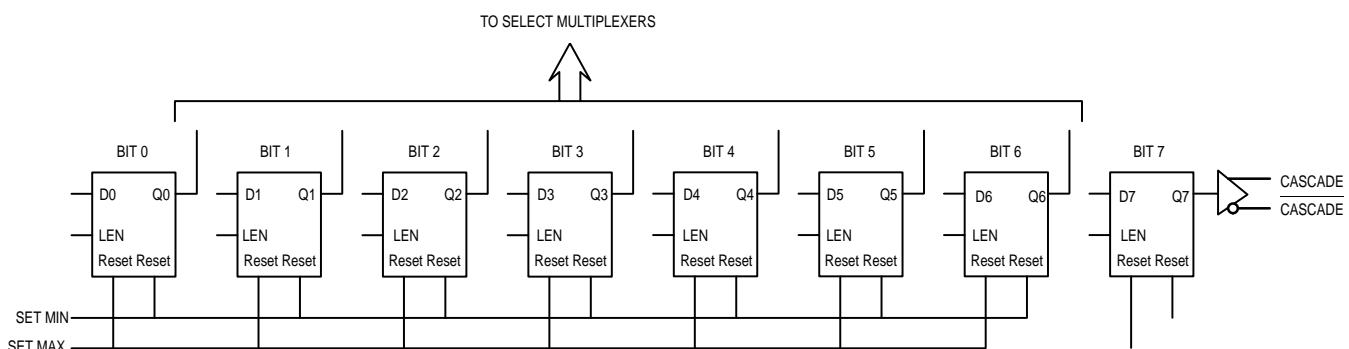
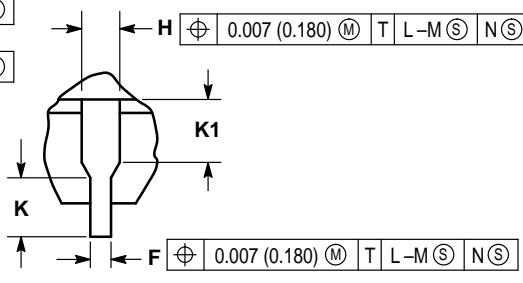
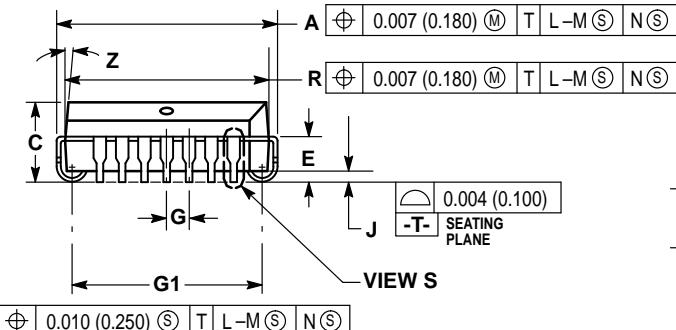
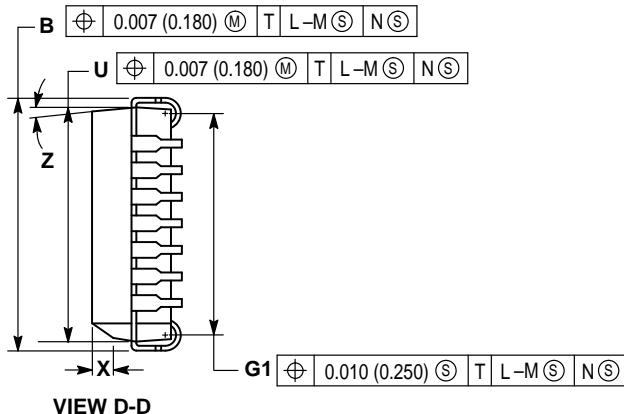
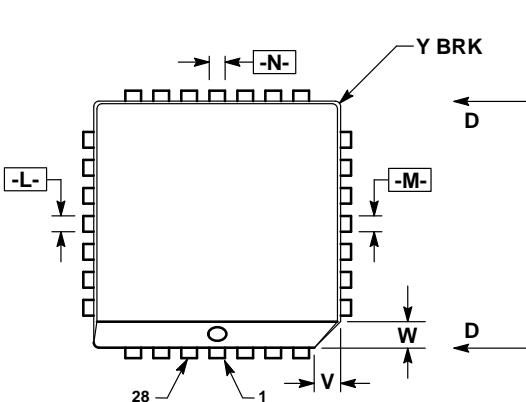


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D



\oplus 0.010 (0.250) \ominus T L-M \ominus N \ominus

NOTES:

1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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